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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/739,506	12/18/2000	Leo Carl Christensen	US000344***	3124

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
BLOUNT, STEVEN	
ART UNIT	**PAPER NUMBER**
2661	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/739,506	CHRISTENSEN, LEO CARL	
	Examiner	Art Unit	
	Steven Blount	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 4/25/05.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1, 3 - 10 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1, 3 - 10 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 3 - 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. patent 3,761,894 to Pile et al in view of U.S. patent 6,208,641 to Ruuskanen et al.

With regard to claim 1, Pile et al teach a circuit for writing data to RAM 110(1), 110(2), etc. (see figure 1) during a first time interval, bit selectors (col 2 line 50 and col 5 line 40) for constructing data streams during a second time interval, the RA comprised of two parts, configured so that a read occurs from a first part while a write occurs to a second part, as described in col 2 lines 32+. Pile et al does not, however, teach the data which is written into the RAM during the first operation to comprise writing "identical images" to the RAM, as required by lines 2+.

Ruuskanen et al teaches, in a similar system, that "During the write phase, the four-bit 8x4M output signal from multiplexers A1 – A4 is written simultaneously into each of the four switching memories under the control of a common write address counter" (col 4, lines 54+). Ruuskanen et al states that this is done to limit the size of the switch and its power consumption. See col 1, lines 43+.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have written identical images of the data into the RAM of Pile et al, light of the teachings of Ruuskanen et al, in order to produce a more compact and power efficient circuit.

With regard to the following claims (hereinafter denoted as "Cl"), note the following: Cl 3: see address bus 107 in Pile et al; Cl 4: note the controller in Ruuskanen et al mentioned above, the output streams mentioned above that are generated, and the split RAM construction mentioned above; Cl 5: note the bus mentioned above; Cl 6: it would be obvious for the bit rate of the outputs to be less than the bit rate of the bus in view of the operation performed by the circuit; Cl 7: time switching is mentioned in the abstract of Pile et al, and with respect to the other claimed features, see the rejection of claim 1 above; Cl 8 – 10: see the rejections above, particularly col 2 lines 32+ of Pile et al.

3. Claim 11 is rejected under 35 U.S.C. 103(a) as being obvious over the Applicants Admitted Prior Art (hereinafter "AAPA) in view of U.S. patent 3,761,894 to Pile et al and U.S. patent 6,208,641 to Ruuskanen et al.

AAPA states, in the background section of the specification, lines 12+, that

"In broadcast systems, video and audio data are transmitted between N originating sources and M destination sinks...The control of a broadcast facility may involve rapid switching between many such sources and sinks...In time multiplexing, all sources and all sinks are connected to the same physical channel...When a switching system grows in terms of the number of sources and sinks it must handle, problems

attend all three different kinds of systems. In time multiplexed systems, the bandwidth of the common physical channel has to be increased in proportion with the number of routes sharing the channel." AAPA then states that "There is a perennial need for switches that handle digital data synchronously, and that must remain time aligned, and that do not grow in complexity too fast as the endpoint capacity of the switch increases."

AAPA does not, however, teach the solution to this problem in the broadcasting systems to comprise writing identical images to memory during a first time interval, and reading them in a second time interval, including the use of bit selectors. This type of a system is taught in Pile et al/Ruuskanen et al, as discussed above. Note also that Ruuskanen et al discusses the motivation behind their invention (which would include the use of multiple RAM memory units that are identically imaged) to be having switches which are of a more compact size for a given amount of data (ie, a greater capacity switch) as discussed in col 1, lines 35 – 47.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have identically imaged and alternately read/written the broadcast data mentioned in AAPA in light of the teachings of Pile et al/Ruuskanen et al in order to provide a switch capable of handling the increased data load associated with broadcast communications.

Response to Arguments

4. Applicant's arguments with respect to the claims have been considered but are not considered persuasive.

The applicant argues that "the Pile reference relates only to time multiplexing. Storage appears to be only after the multiplexing and selection process occurs."
In response, the examiner notes that Ruuskanen et al has the time division multiplexed data which are stored in the memory. See the abstract, lines 3+. Likewise, Pile also deals with data which is time division multiplexed prior to its storage in memory. See the abstract, columns 7+.

Applicant states that Pile is not compatible with bit selection. The examiner notes, however, that bit selection is taught in col 6 lines 35+ : "For reasons described in detail hereinafter, the designation of each channel preferably occurs during the byte interval assigned to the immediately preceding outgoing channel. Output leads s(1) to s(5) extend in parallel to memory and logic circuits 110(1) through 110(P) to provide the address of the channel assigned to the next subsequent byte interval. Thereafter, during this next byte interval, any byte stored in a memory set in the storage area dedicated to the channel, is read out to the outgoing line."

The examiner notes that it is commonly known in a digital telephony system (ie, employing a PCM) to use multicasting. See, for example, US Patent Number 4,301,531 to Lubin.

The examiner notes that Ruuskanen et al state in col 2 lines 20+ that it is *preferable* that the signals are stored by writing the bits of the serial signals into the same memory location having a width of several bits.

The examiner finally notes that reading and writing simultaneously to/from several memory elements is well known in the art. See, for example, US Patent 3,967,070 to Srivastava et al and US patent 4,905,226 to Kobayashi.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Blount whose telephone number is 571 - 272 - 3071. The examiner can normally be reached on M-F 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Chau Nguyen, can be reached on 571 – 272 - 3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ajit Patel
Primary Examiner

SB
7/4/05